A DOCPHOENIX

OUTGOING DOCUMENT INDEX SHEET

OUTGOING

_____ CTMS _____
Miscellaneous Office Action

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Miscellaneous Internal Document

_____ NRES _____
Letter Requiring Period for Response

_____ 1449 _____
Signed 1449

_____ 892 _____
892

_____ ABN _____
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_____ APDEC _____
Board of Appeals Decision

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Examiner Answer to Appeal Brief

_____ CRFR _____
Letter Requiring CRF

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Foreign Reference

_____ M903 _____
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_____ M905 _____
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OUTGOING

_____ NFDR _____
Formal Drawing Required

_____ NOA _____
Notice of Allowance

_____ NPL _____
Non-Patent Literature

_____ PEFN _____
Pre-Exam Formalities Notice

_____ PETDEC _____
Petition Decision

PTO INTERNAL

_____ CLMPTO _____
PTO Prepared Complete Claim Set

_____ IIFW _____
File Wrapper Issue Information

_____ SRNT _____
Examiner Search Notes

_____ SRFW _____
File Wrapper Search Info

4/25/03

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/486,556	02/29/2000	NOBUAKI HASHIMOTO	105029	8629

25944 7590 08/13/2003

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/486,556	HASHIMOTO, NOBUAKI	
	Examin r	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 68-71, 73-77, 79 and 82-85 are rejected under 35 U.S.C. 102(e) as being anticipated by Imasu et al., US Patent No. 6,208,525, hereafter Imasu.

Regarding claim 68, 82 and 84, Imasu discloses a semiconductor device, comprising:

a substrate (wiring board 1, see figure 1 and 2 and 11, column 4, line 1-25),

said substrate having an interconnect pattern formed there over (see figure 2 and 11),

said substrate having a protective layer covering at least a part of said interconnect pattern (passivation film 5 and 6, see figure 2 and 11, column 4, line 40-50);

a semiconductor chip said semiconductor chip having electrodes, said electrodes electrically connected to said interconnect pattern, said semiconductor chip mounted on said substrate such that an edge of said semiconductor chip does not overlap with said protective layer (semiconductor chip 10, see figure 2 and 11); and

an adhesive, said adhesive adhering said semiconductor chip to said substrate, said adhesive provided on said substrate from a region in which said semiconductor chip is mounted to said protective layer, wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat (adhesive 16, see figure 2 and 11, column 4, line 55-60).

Regarding claim 74, 83 and 85, Imasu discloses all the features of the claimed invention as applied to claim 68 above including adhesive between the substrate and the semiconductor chip, see figure 2, 11).

Regarding claim 69 and 75, Imasu further discloses an anisotropic adhesive (column 8, line 1-10).

Regarding claim 70 and 76, Imasu further discloses anisotropic conductive cover whole of said interconnect pattern (figure 2 and 11).

Regarding claim 71 and 77, Imasu further discloses the adhesive covering part of a lateral surface of said semiconductor chip (see figure 2 and 11).

Regarding claim 73 and 79, Imasu further discloses the protective layer cover said substrate except said region in which said semiconductor chip is mounted and a periphery of said region (passivation film 5 and 6, see figure 2 and 11, column 4, line 40-50).

1. Claims 72 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imasu et al., US Patent No. 6,208,525, hereafter Imasu, as applied to claims 68-71, 73 and 74 to 77 and 79 above, and further in view of Shigeki, Japanese Patent JP356050546A.

Regarding claims 72 and 78, the applicant is claiming a shading material added to the adhesive. Though, Imasu does not disclose such shading, shading is known in the art and can be used depending upon the specific requirement for shielding the semiconductor die from light rays. Shigeki disclose discloses such light shielding resin for protecting the chip from malfunctioning and damage. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the assembly of Imasu with shading material added in the adhesive in order to shielding the chip from light. Further, it has been held to be within the general skill of a

worker in the art to select a known material on the basis of its suitability for the intended use as matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

2. Claims 30-67, 80-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imasu et al., US Patent No. 6,208,525, hereafter Imasu and Shigeki, Japanese Patent JP356050546A, as applied to claims 68-79 above and Higashi et al., US Patent 5,918,113, here after Higashi.

Regarding claims 30-67, the applicant is claiming the method of manufacturing a semiconductor device. The combination of Imasu and Shigeki discloses the all the limitation of the product as claimed and the method steps are inherent and obvious, if not identical, in view of the product claims.

Regarding claim 80 and 81, the applicant is claiming the semiconductor devices by the method as defined in claims 30 and 50, respectively. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentability distinguish the product over the prior art, in the case that the product is the same or obvious over, the prior art, See Product-by-Process in MPEP 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

Response to Arguments

3. Applicant's arguments filed on May 6, 2003 have been fully considered but they are not persuasive. (a) Applicant's argument: Figure 2, shows the existence of passivation film 5.

The embodiment with figure 11 is not showing the passivation layer and is applied for the rejection, see column 8, line 25-27. Reference of figure 2 is made in the rejection as the complete description is not there for figure 11. Instead only the changes are described for embodiment of figure 11.

(b) Applicant's argument: New limitation, "wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain ***substantially flat***", is not disclosed by the prior art of Imasu.

According to Amendment of May 6, 2003, figure 2B, support the new limitation and according to supplemental remarks, Figure 4B support the new limitation.

However, nothing is disclosed or described in the specification about the flatness of the substrate.

Further, as seen in the figure 11 of the applied prior art of Imasu, in comparison to the total thickness of the substrate, the surface of the substrate is considerably flat, even after small recess formed by elastic deformation of the electrode pads.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Otani et al., disclose a semiconductor chip mounted on a substrate with a protective layer wherein the semiconductor chip does not overlap with the protective layer, see figure 1 and 4.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (8:30 - 5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.